REMARKS

The application has been reviewed in light of the Office Action mailed February 24, 2005. Reconsideration is respectfully requested in light of the following remarks.

Claims 82, 83 and 85 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Office Action asserts that in claim 82 the limitation "'at least one brace comprises a plurality of braces' is not described in the specification and shown in the figure because there is only one brace (690) in figure 6E." Office Action, page 2. The Office Action also asserts that in claim 85, the limitation "'a plurality of brace[s] transversely extending between lateral sides of at least two of the free-standing microstructures' is not described in the specification and shown in the figure because there is only one brace (690) in figure 6E." Id.

Applicants respectfully disagree. Although Figure 6E shows one brace extending between adjacent sides of conductive studs 68, Applicants expressly stated in the specification that the invention is not so limited, and disclosed examples of the embodiments recited in claims 82, 83 and 85. For example, the specification discloses that "it is also possible to provide more than one dielectric brace layer where they intersect at a container (or containers) such that a two-dimensional network or lattice of dielectric brace layers is formed through-out the array of containers." Specification, page 8, lines 25-28. Thus, the written description requirement is met because "the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed." MPEP § 2163.02.

The Office Action is silent as to why claim 83 is rejected under written description requirement. Claim 83 recites the "semiconductor support structure of claim 82, wherein said plurality of braces form a lattice support structure." Claim 83 plainly satisfies the written description requirement based at least on the specification passage quoted above. Applicants note that this is the only rejection of claims 82 and 83, and, as such, claims 82 and 83 are considered to be in condition for allowance.

Claims 1-3, 5, 6, 8, 9, 11, 13, 23, 28, 39, 44, 78-81 and 85 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Liu et al., U.S. Patent No. 6,037,216 ("Liu"). Reconsideration is respectfully requested for the following reasons.

Claim 1 recites a semiconductor device comprising a "a plurality of upright free-standing microstructures formed over the substrate; and a brace transversely extending between lateral sides of at least two of the free-standing microstructures." Liu fails to teach or suggest "free-standing microstructures," or a "brace transversely extending between lateral sides of at least two of the free-standing microstructures."

The free-standing micro structures are described, for example, with reference to Figures 6A-6E and pages 11-12 of the specification. In an exemplary embodiment, via holes 67 are formed in dielectric layer 66, and are then filled with conductive material to form conductive studs 68. "The second dielectric layer 66 is then selectively etched ... [, and a] free standing stud structure 68 is left exposed ... ." Specification, page 12, lines 11-13.

The Office Action asserts that Liu teaches a "plurality of free-standing microstructures (39) formed over the substrate (1)." Office Action, page 3. Liu provides no basis for this assertion. Liu teaches etching openings 37b through multiple layers of its device, and then filling the openings 37b with storage node structures 39. Column 6, line 45 through column 7, line 15. Nothing in Liu teaches or suggests processing its device such that storage nodes 39 form "free-standing microstructures." For at least this reason claim 1 is allowable over Liu.

Moreover, Liu fails to teach or suggest a "brace transversely extending between lateral sides of at least two of the free-standing microstructures." An exemplary embodiment of the claimed "brace" is illustrated and described in Figures 6C-6E, and page 12 of the specification. According to the specification, the "dielectric brace layer ... is deposited to prevent falling of tall containers ... ." Specification, page 8, line 3. "A free standing stud structure 68 is left exposed with transverse structural support from brace

layer 690 ... after removing the second dielectric layer 66." Specification, page 8, lines 20-22. "In this way, the studs 68 are afforded good mechanical support in at least the transverse or lateral directions during removal of the second dielectric 66 and further wafer handling and processing operations." Specification, page 12, lines 28-30.

The Office Action asserts that Liu teaches a "brace (33) transversely extending between ... the free-standing microstructures (39)." Office Action, page 3. Liu provides no support to this assertion. Element 33 in Liu is a silicon nitride layer which is deposited over a silicon oxide layer 32. Nowhere does Liu teach or suggest that the silicon nitride layer 33 is a "brace," or a type of structure that provides mechanical support in the transverse or lateral directions. Rather, Liu's silicon nitride layer 33 is used for patterning and aligning openings in an underlying layer. Column 6, lines 36-44. Thus, Liu fails to teach or suggest a "brace transversely extending between lateral sides of at least two of the free-standing microstructures." For this additional reason, claim 1 is allowable over Liu.

Claims 2, 3, 5, 6, 8, 9, 11 and 13 depend from claim 1 and contain every limitation of claim 1. These dependent claims are allowable for at least the reasons for allowance of claim 1, and also because the unique combinations recited in the dependent claims are neither taught nor suggested by Liu.

Claim 23 recites, inter alia, a "plurality of upright free-standing capacitor storage node microstructures formed over the substrate; and a brace transversely extending between lateral sides of at least two of the free-standing microstructures." Claim 28 recites, inter alia, a "plurality of upright free-standing capacitor storage node microstructures formed over the substrate; and a brace transversely extending between lateral sides of at least two of the free-standing microstructures." Claim 39 recites, inter alia, a "plurality of upright free-standing capacitor storage node microstructures ...; and a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures." Claim 44 recites, inter alia, a "plurality of upright free-standing capacitor storage node microstructures ...; and a brace transversely

extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures."

Claim 78 recites, inter alia, a "plurality of braces transversely extending between lateral sides of a plurality of microstructures ..., wherein said plurality of braces comprise a support structure for said plurality of microstructures." Claim 79 recites, inter alia, "at least one brace transversely extending between lateral sides of at least two of a plurality of microstructures on a semiconductor substrate, wherein said at least two of said plurality of microstructures are supported only by said at least one brace." Claim 80 recites, inter alia, "at least one brace transversely extending between lateral sides of at least two of said plurality of microstructures, wherein said at least two of said plurality of microstructures are supported only by said at least one brace." Claim 81 recites, inter alia, "at least one brace transversely extending between lateral sides of at least two of the microstructures, wherein the brace comprises a support structure." And, claim 85 recites, inter alia, a "plurality of braces transversely extending between the vertical surfaces of at least two of the microstructures."

As discussed above with respect to claim 1, Liu fails to teach or suggest the above-quoted limitations of claims 23, 28, 39, 44, 78-81 and 85. Claims 23, 28, 39, 44, 78-81 and 85 are thus allowable over Liu.

Claim 77 stands rejected as being unpatentable over Liu in view of Sandhu et al., U.S. Patent No. 6,303,956 ("Sandhu"). This rejection is respectfully traversed for the following reasons.

Claim 77 recites a "plurality of upright free-standing capacitor storage node microstructures ...; and a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures." As discussed above with respect to claim 1, Liu fails to teach or suggest these claim limitations. The Office Action does not rely on Sandhu for these limitations, and Sandhu does not teach or

suggest these limitations. Thus, Liu and Sandhu, taken alone or in combination, fail to teach or suggest the limitations of claim 77, and claim 77 is allowable.

Moreover, this rejection should be withdrawn because Sandhu is not a proper reference under 35 U.S.C. § 103(c), which provides that "[s]ubject matter developed by another person, which qualifies as prior art only under one or more subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

This is the case here. The subject application has an effective filing date of August 31, 1999. Sandhu was developed by "another person," and was filed on February 26, 1999 and issued on October 16, 2001. Thus, Sandhu qualifies as prior art only under 102(e). And, at the subject matter of Sandhu and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to the same person – Micron Technology, Inc. Therefore, Sandhu is not a proper reference under § 103. This is an additional reason for allowance of claim 77.

Claim 84 stands rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,667,502. Applicants are submitting herewith a terminal disclaimer to overcome the rejection. Thus, claim 84 is in condition for allowance.

Applicants note with appreciation the indication that claim 10 would be allowed if rewritten in independent form. Claim 10 is believed to be allowable in its present form due to its dependence upon claim 1, which is allowable over Liu as discussed above.

On a separate matter, Applicants respectfully request that withdrawn claim 4 be examined in the application. In the Response to Election of Species Requirement filed on December 3, 2004, Applicants elected the Embodiment of Figure 6E, but omitted claim 4 from the list of claims readable on the elected embodiment. Claim 4 recites the

"semiconductor device according to claim 1, wherein the brace has a width approximately equal to or less than the largest cross-sectional dimension of the microstructures." This feature of the invention, discussed on page 9, lines 1-6 of the specification, for example. Claim 4 is readable on the elected embodiment of Figure 6E. Claim 4 is believed to be allowable because the prior art of record fails to teach or suggest that the "brace has a width approximately equal to or less than the largest cross-sectional dimension of the microstructures."

In view of the above remarks, Applicants believe that the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Peter A. Veytsman
Registration No.: 45,920
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant